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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,968	01/29/2004	Dominique Mangelinck	ASTAP2004-01	1967

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HORIZON IP PTE LTD
8 KALLANG SECTOR, EAST WING
7TH FLOOR
SINGAPORE 349282, 349282
SINGAPORE

EXAMINER
SARKAR, ASOK K

ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,968	MANGELINCK ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 18, 2007 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1 – 41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 21, 23 – 25, 27 – 30, 32 – 34, 36 – 38 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Bai, US 6,204,103.

Regarding claim 1, Bai teaches a method of fabricating a gate electrode for a semiconductor comprising the steps of:

- providing a substrate 1601 (Fig. 17);

- providing a substrate prepared with a gate stack, the gate stack includes a gate dielectric 120 on the substrate and a gate layer 1602 on the gate dielectric 120, the gate layer comprising a first material of thickness t_p , the first material being selected from the group consisting of Si (column 6, lines 33 – 47) ;
- providing a layer of metal of thickness t (Fig. 17); and
- annealing the layers, such that all of the first material of the gate material and substantially all of the metal layer over the gate layer are consumed during reaction with one another (Fig. 18) in column 6, lines 51 – 62 to form a resulting layer which serves as a ate electrode in contact with the gate dielectric 120 wherein the gate electrode comprises a work function close to about a mid – gap of silicon band gap (column 2, lines 6 – 22) with reference to Figs. 13 and 18 and in between column 6, line 63 and column 7, line 5.

Regarding claims 2 and 25, Bair teaches the metal Ti in column 6, line 63.

Regarding claim 3, Bai teaches the gate stack further comprises dielectric sidewall spacers 150 (Fig. 14) and providing the metal layer comprises depositing the metal layer on the first material layer with reference to Fig. 17.

Regarding claims 4 and 5, Bai teaches the thicknesses t_p and t_m are related by a predetermined ratio of t_m /t_p and the ratio is determined by the first material and the metal since sometimes the reaction does not consume all of the metal.

Regarding claim 6, Bai teaches annealing is performed at temperatures ranging from 300 to 900°C in column 7, line 1.

Regarding claim 7, Bai teaches the step of depositing a further layer of metal (Mo) on the gate electrode to increase gate thickness with reference to Fig. 17.

Regarding claim 8, Bai teaches forming source/drain contacts 18 simultaneously with the gate electrode with reference to Fig. 14.

Regarding claim 9, Bai teaches as much as 5% of the metal remains following reaction with the other of the metal and the first material in column 7, lines 1 – 5. (The remaining metal, if any, inherently means lass than about 5%).

Regarding claim 10, Bai teaches the gate electrode for a semiconductor device comprising a substrate with a gate stack formed thereon, the gate stack includes a gate dielectric on the substrate and a gate electrode on the gate dielectric, wherein the gate electrode comprises a first material and a metal, which have been substantially consumed during reaction with one another caused by annealing with reference to Figs 17 and 18 as was described earlier in rejecting claim 1.

Regarding claims 11 and 12, Bai teaches these limitations as was described earlier in rejecting claims 1 and 2.

Regarding claim 13, Bai teaches as much as 5% of the metal remains following reaction with the other of the metal and the first material as was described earlier in rejecting claim 9.

Regarding claim 14, Bai teaches the step of depositing a layer of metal on the gate electrode as was described earlier in rejecting claim 7.

Regarding claim 15, Bair teaches the gate electrode is incorporated in a CMOS semiconductor device in column 1, lines 52 – 62.

Regarding claims 16, 18 and 19, Bai teaches all limitations of the claim as described earlier in rejecting claims 1 – 9. The metal silicide materials such as $TiSi_2$ or $MoSi_2$ inherently have the work functions close to the mid – gap energy of semiconductor material such as silicon (column 2, lines 6 – 22). The reduction of problems associated with inversion and agglomeration associated with formation of the transistor is inherent.

Regarding claim 17, Bai teaches the substrate is prepared with at least first and second gate stacks with dielectric sidewall spacers on the substrate and first and second diffusion regions in the substrate adjacent to the gate stacks, the gate stacks include a gate dielectric on the substrate and a gate layer on the gate dielectric, the first and second gate stacks serving as a first PMOS transistor and a first NMOS transistor to form a CMOS integrated circuit; and the material of the first layer comprises silicon as was described earlier in rejecting claims 1 and 15. The formation of two gates with two gate stacks, sidewall pacers and diffusion regions are inherent in the methods of preparing PMOS and NMOS parts of the CMOS transistor.

Regarding claims 20, 23, 27, 28, 30, 32, 34, 36, 38 and 40, Bair teaches annealing in column 6, line 67.

Regarding claims 21 and 24, Bai teaches unreacted metal layer is less than or equal to 10% in column 7, lines 1 – 5. (The remaining metal, if any, inherently means lass than about 10%).

Regarding claims 29 and 37, Bai teaches the first layer comprises a first thickness t_p and the metal layer comprises a second thickness t_m, and wherein a

minimum of a ratio of the first and second thickness t_p/t_m results in consumption of substantially the first gate and metal layers during processing of the metal layer as shown in Figs. 6 – 8 and associated descriptions in the disclosure.

Regarding claim 33, Bai teaches etching remaining portion of unreacted metal layer above the gate electrode after processing the metal layer in column 7, lines 1 – 5.

Regarding claim 41, Bai teaches an integrated circuit comprising a transistor disposed on a substrate, the transistor having a gate stack with a gate dielectric disposed on the substrate and a gate electrode disposed on and in contact with the gate dielectric, and first and second diffusion regions adjacent to the gate stack, the gate electrode is formed from an amorphous or polycrystalline first layer and a metal layer in which all of the first layer and all of the metal layer have been substantially consumed during reaction with one another caused by annealing, wherein problems associated with inversion and agglomeration associated with formation of the transistor is reduced with reference to Fig. 18. This is a product by process claim.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 22, 26, 31, 35, 39 and 42 rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner, US 6,100,173 in view of Bai, US 6,204,103.

Regarding claims 22, 26, 31, 35 and 39, Gardener teaches metal layer forms silicide over the diffusion regions with reference to Figs. 10 – 12. Gardener teaches all

limitations of claims 16, 25, 29, 34 and 37, but fails to teach the step of processing the metal layer to cause a reaction between the gate layer and the metal layer such that substantially all the material of the gate layer and portions of the metal layer over the gate layer are consumed to form a resulting layer having a work function close to a mid gap of silicon band gap which serves as the gate electrode which contacts the gate dielectrics.

Bai teaches forming CMOS devices in which he teaches the step of processing the metal layer to cause a reaction between the gate layer and the metal layer such that substantially all the material of the gate layer and portions of the metal layer over the gate layer are consumed to form a resulting layer with reference to Figs. 17 and 18 having a work functions of 4.1 eV and 5.1 eV (column 6, lines 32 – 67) which are inherently close to a mid gap of silicon band gap which serves as the gate electrode which contacts the gate dielectrics for the benefit of maintaining symmetry between NMOS and PMOS devices and other additional benefits in column 2, lines 6 – 22.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Gardner and process the metal layer to cause a reaction between the gate layer and the metal layer such that substantially all the material of the gate layer and portions of the metal layer over the gate layer are consumed to form a resulting layer having a work function close to a mid gap of silicon band gap for the benefit of maintaining symmetry between NMOS and PMOS devices and other additional benefits as taught by Bai in column 2, lines 6 – 22.

7. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, US 6,555,438 in view of Bai, US 6,204,103.

Wu teaches a method of fabricating a gate electrode for a semiconductor comprising the steps of:

- providing a substrate prepared with a gate stack 12, the gate stack includes a gate dielectric 10 on the substrate 2 and a gate layer 12 on the gate dielectric 10, the gate layer comprising a first material of thickness t_p, the first material being selected from the group consisting of Si with reference to Figs. 1 and 2 in column 4, lines 14 – 62;
- providing a metal layer 26 on the gate layer 12, the metal layer having a thickness t_m with reference to Fig. 7; and
- annealing the layers, to form a resulting layer which serves as the gate electrode in contact with the gate dielectric, wherein source/drain contacts are formed simultaneously with the gate electrode with reference to Fig. 8 in between column 5, line 50 and column 6, line 20.

Wu fails to teach annealing the layer such that substantially all of the first material of the gate layer and metal of the metal layer over the gate layer are consumed during reaction with one another.

Bai teaches forming CMOS devices in which he teaches the step of annealing the layer such that substantially all of the first material of the gate layer and metal of the metal layer over the gate layer are consumed during reaction with one another with reference to Figs. 17 and 18 having a work functions of 4.1 eV and 5.1 eV (column 6,

lines 32 – 67) for the benefit of making mid – bandgap metal gate electrodes having Fermi level selected midway between the Fermi level of NMOS and PMOS devices to maintain symmetry between NMOS and PMOS devices and other additional benefits in column 2, lines 6 – 22.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Wu and anneal the layer such that substantially all of the first material of the gate layer and metal of the metal layer over the gate layer are consumed during reaction with one another for the benefit of making mid – bandgap metal gate electrodes having Fermi level selected midway between the Fermi level of NMOS and PMOS devices to maintain symmetry between NMOS and PMOS devices and other additional benefits as taught by Bai in column 2, lines 6 – 22.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Asok K. Sarkar
May 30, 2007

Primary Examiner